BUK752R3-40C; BUK7E2R3-40C

N-channel TrenchMOS standard level FET

Rev. 02 — 10 August 2006 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package, using Philips Ultra High-Performance (UHP) automotive TrenchMOS technology.

1.2 Features

- TrenchMOS technology
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

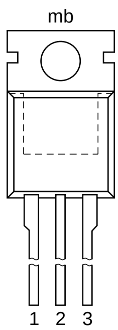
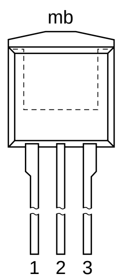
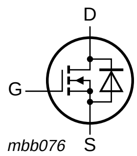
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.2$ J
- $I_D \leq 100$ A
- $R_{DSon} = 1.96$ mΩ (typ)
- $P_{tot} \leq 333$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline		Symbol
1	gate (G)			
2	drain (D)			
3	source (S)			
mb	mounting base; connected to drain			
		SOT78 (TO-220AB)	SOT226 (I2PAK)	

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK752R3-40C	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78
BUK7E2R3-40C	I2PAK	plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB	SOT226

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	40	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-	±20	V
I_D	drain current	V_{GS} = 10 V; see Figure 2 and 3	[1]			
		limited by power dissipation at T_{mb} = 25 °C	[2]	-	276	A
		limited by package at T_{mb} = 25 °C	[1][3]	-	100	A
		limited by package at T_{mb} = 100 °C	[1][3]	-	100	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3		-	1104	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1		-	333	W
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current	T_{mb} = 25 °C	[1]			
		limited by power dissipation	[2]	-	276	A
		limited by package	[3]	-	100	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs		-	1104	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 100 A; V_{DS} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C		-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4]	-	-	J

[1] Refer to document *9397 750 12572* for further information.

[2] Current is limited by chip power dissipation rating.

[3] Continuous current is limited by package.

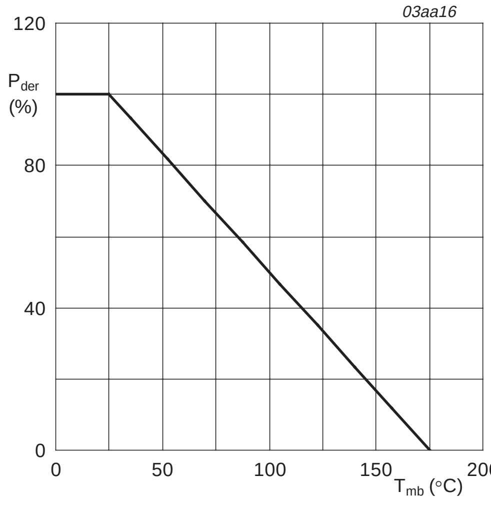
[4] Conditions:

a) Maximum value not quoted. Repetitive rating defined in Figure 16.

b) Single-pulse avalanche rating limited by $T_{j(max)}$ of 175 °C.

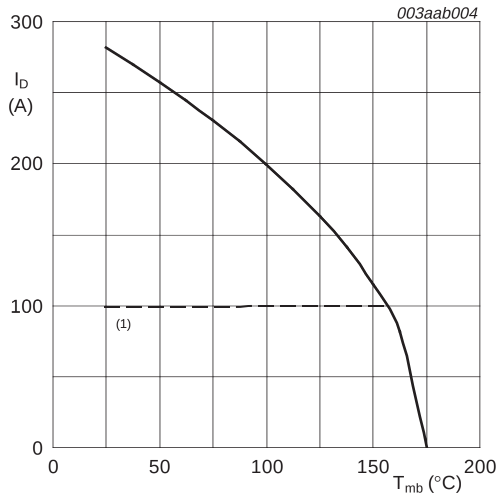
c) Repetitive avalanche rating limited by an average junction temperature of 170 °C.

d) Refer to application note *AN10273* for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

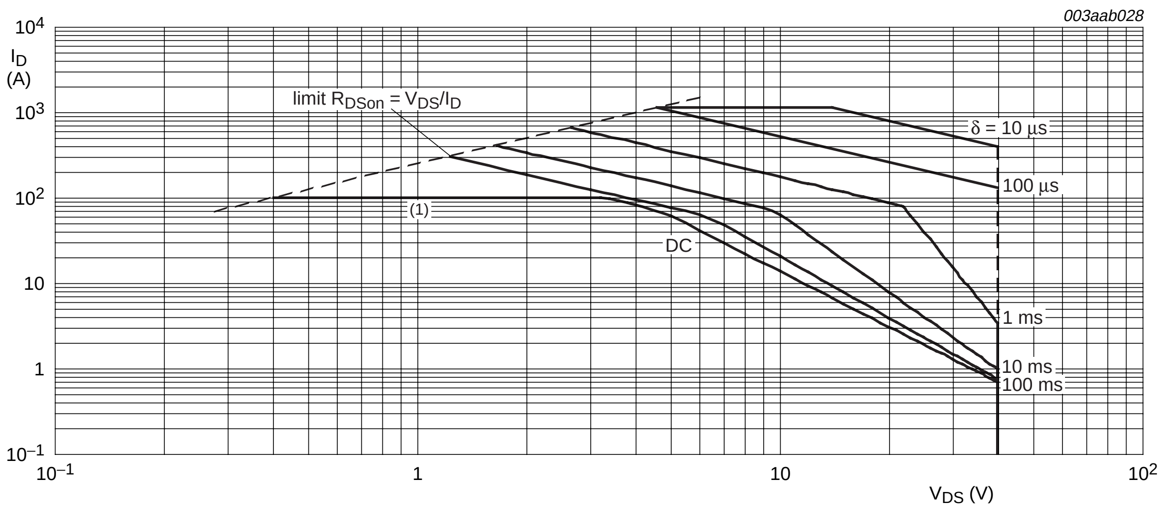
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

(1) Capped at 100 A due to package.

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse.

(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in free air	-	60	-	K/W
	SOT226	vertical in free air	-	50	-	K/W

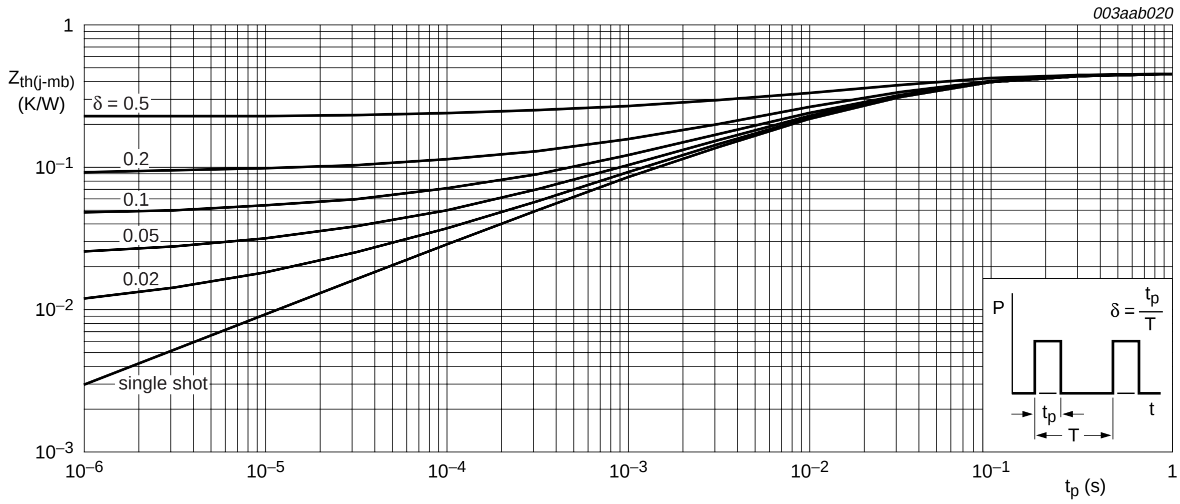


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

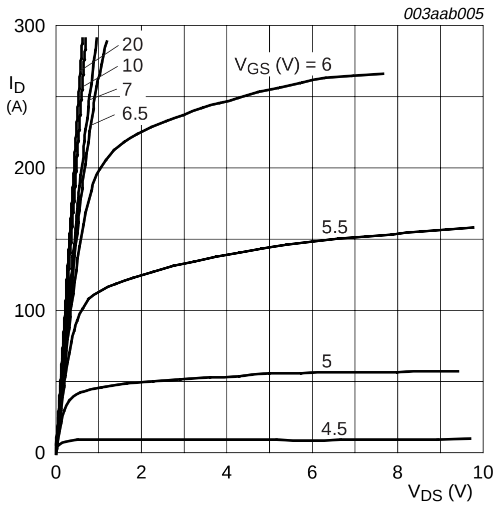
Table 5. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	40	-	-	V
		T_j = –55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; see Figure 6 and 8				
		T_j = 25 °C	-	1.96	2.3	mΩ
		T_j = 175 °C	-	-	4.26	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DD} = 32 V; V_{GS} = 10 V; see Figure 14	-	175	-	nC
Q_{GS}	gate-source charge		-	49	-	nC
Q_{GD}	gate-drain charge		-	67	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	5	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	8492	11323	pF
C_{oss}	output capacitance		-	1606	1927	pF
C_{rss}	reverse transfer capacitance		-	1101	1508	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	65	-	ns
t_r	rise time		-	133	-	ns
$t_{d(off)}$	turn-off delay time		-	146	-	ns
t_f	fall time		-	119	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT226	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH

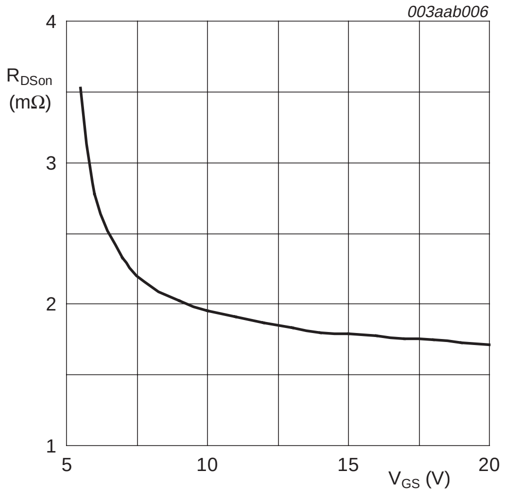
Table 5. Characteristics *...continued*
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	75	-	ns
Q_r	recovered charge		-	57	-	nC



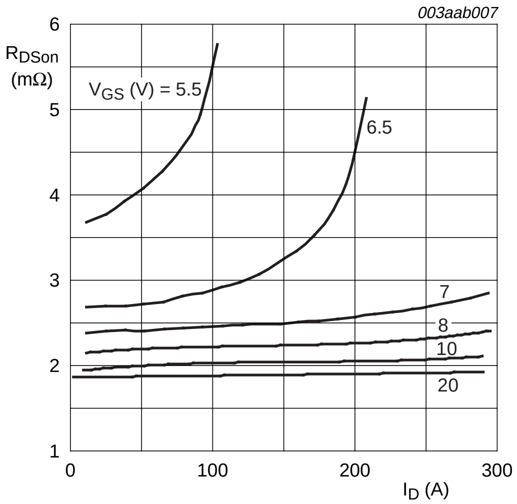
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



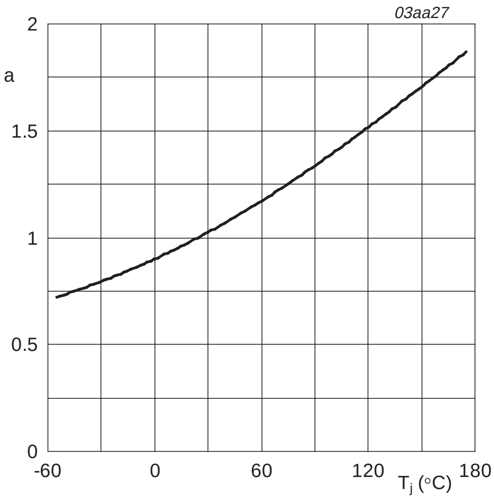
T_j = 25 °C; I_D = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



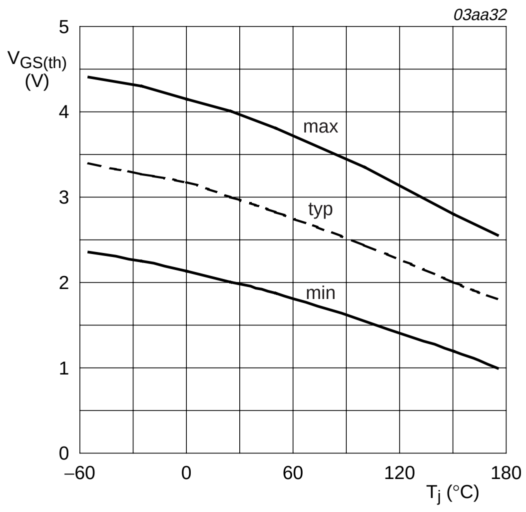
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



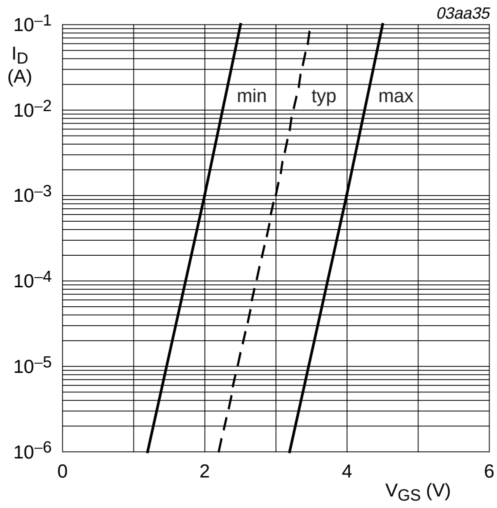
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



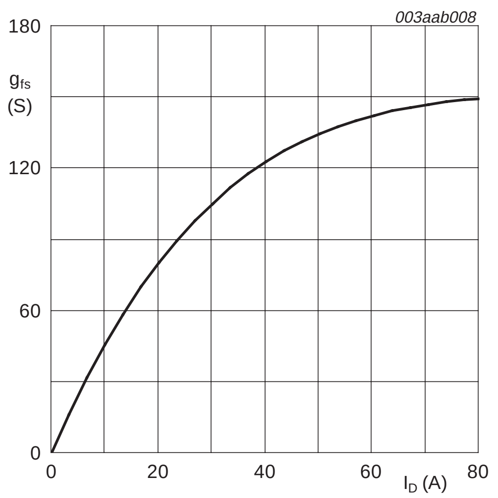
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



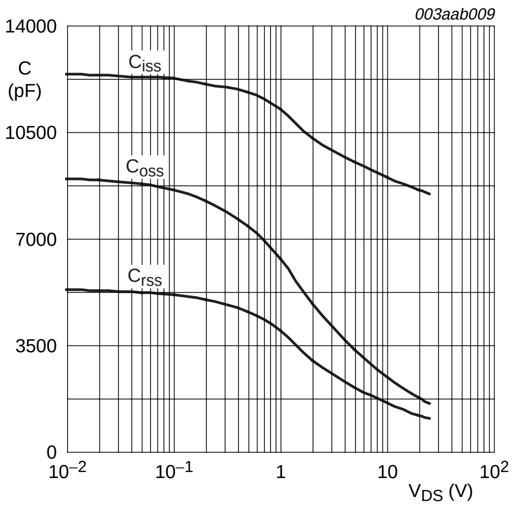
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage



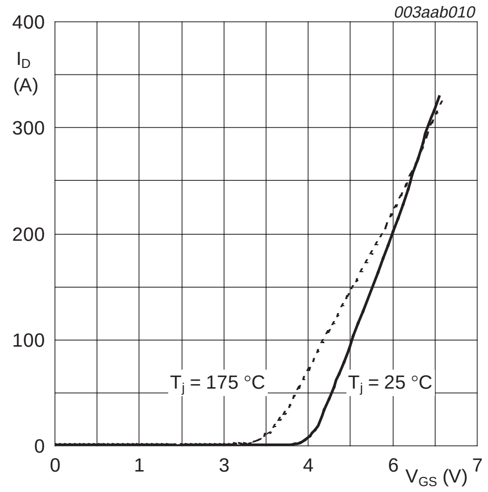
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values



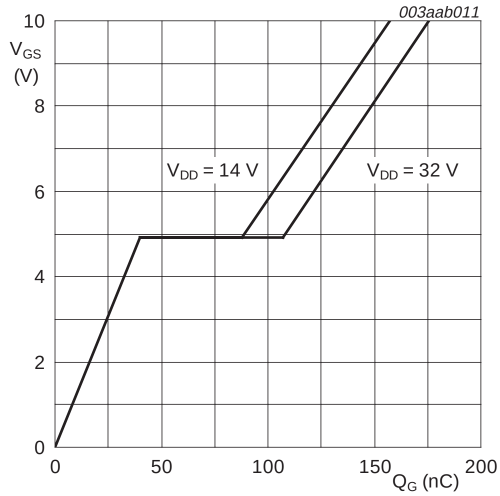
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



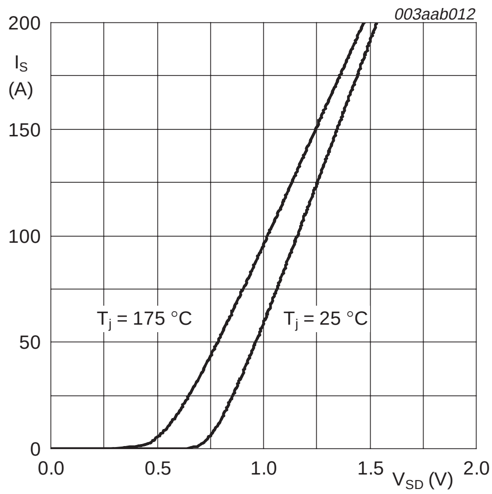
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



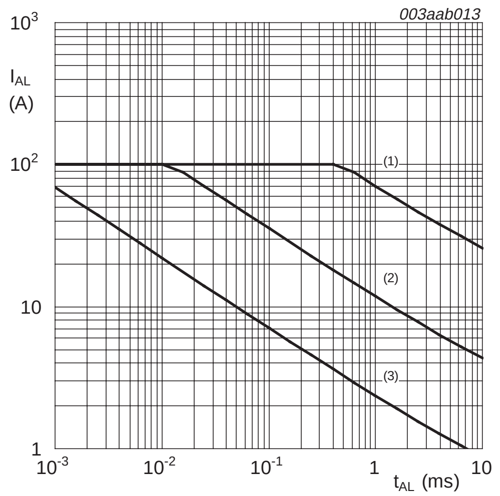
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V

Fig 15. Source current as a function of source-drain voltage; typical values



See Table note 4 of Table 3 “Limiting values”.

(1) Single-pulse; T_j = 25 °C.

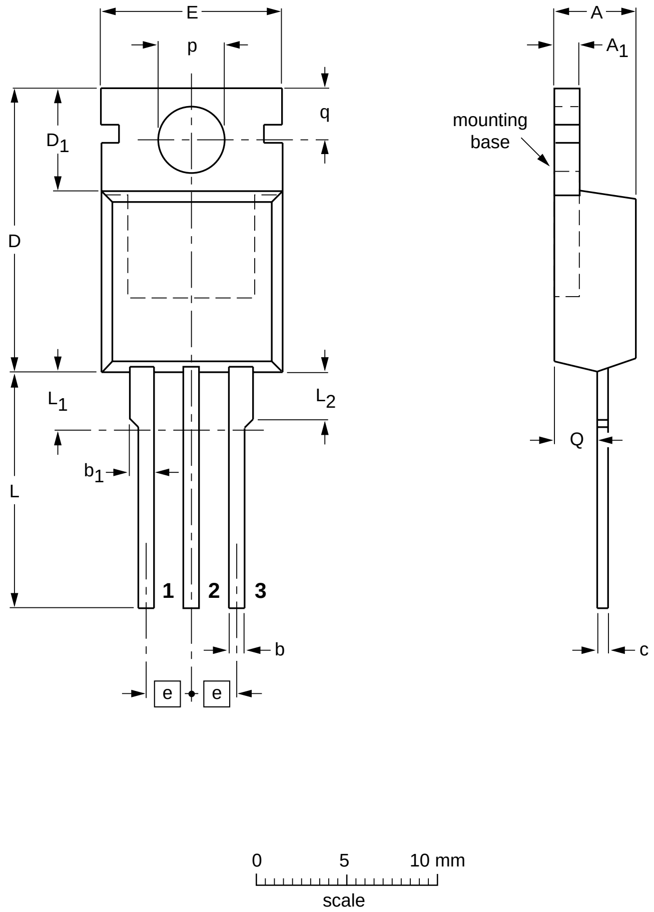
(2) Single-pulse; T_j = 150 °C.

(3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	L_2 max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.45 1.00	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

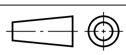
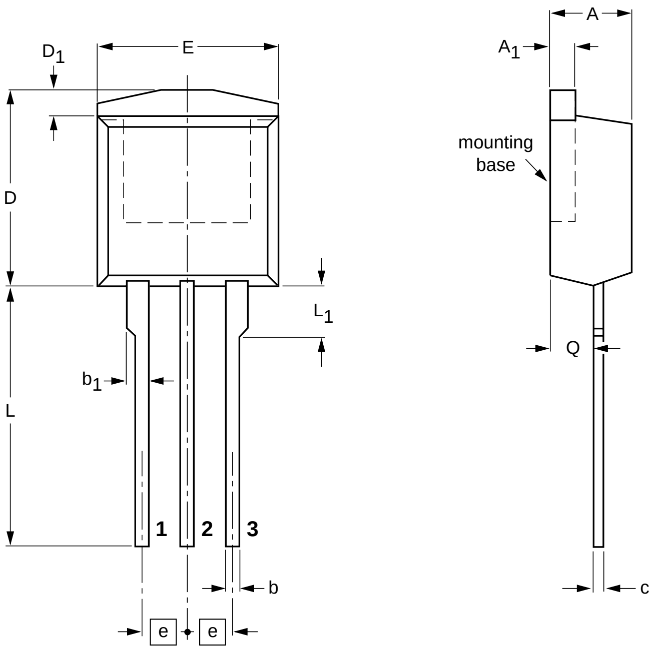
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~05-03-22~~ 05-10-25

Fig 17. Package outline SOT78 (TO-220AB)

Plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D max	D_1	E	e	L	L_1	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	1.3 1.0	0.7 0.4	11	1.6 1.2	10.3 9.7	2.54	15.0 13.5	3.30 2.79	2.6 2.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT226		low-profile 3-lead TO-220AB				~~05-06-23~~ 06-02-14

Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK75_7E2R3-40C_2	20060810	Product data sheet	-	BUK75_7E2R3-40C_1
Modifications:	• Section 6 “Characteristics” correction to Q_{GS} value.			
BUK75_7E2R3-40C_1	20060503	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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11. Contents

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